

FIG. 1

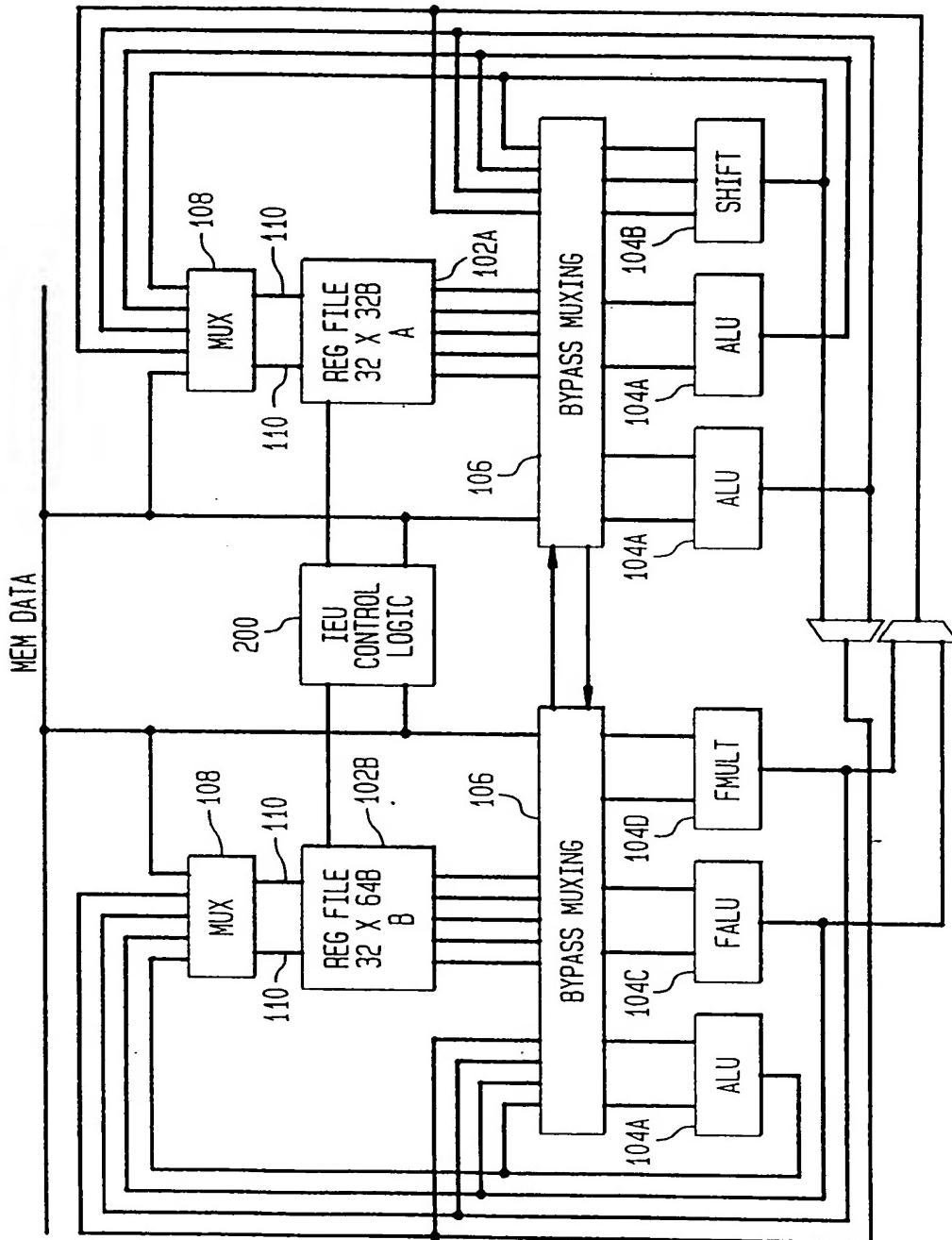
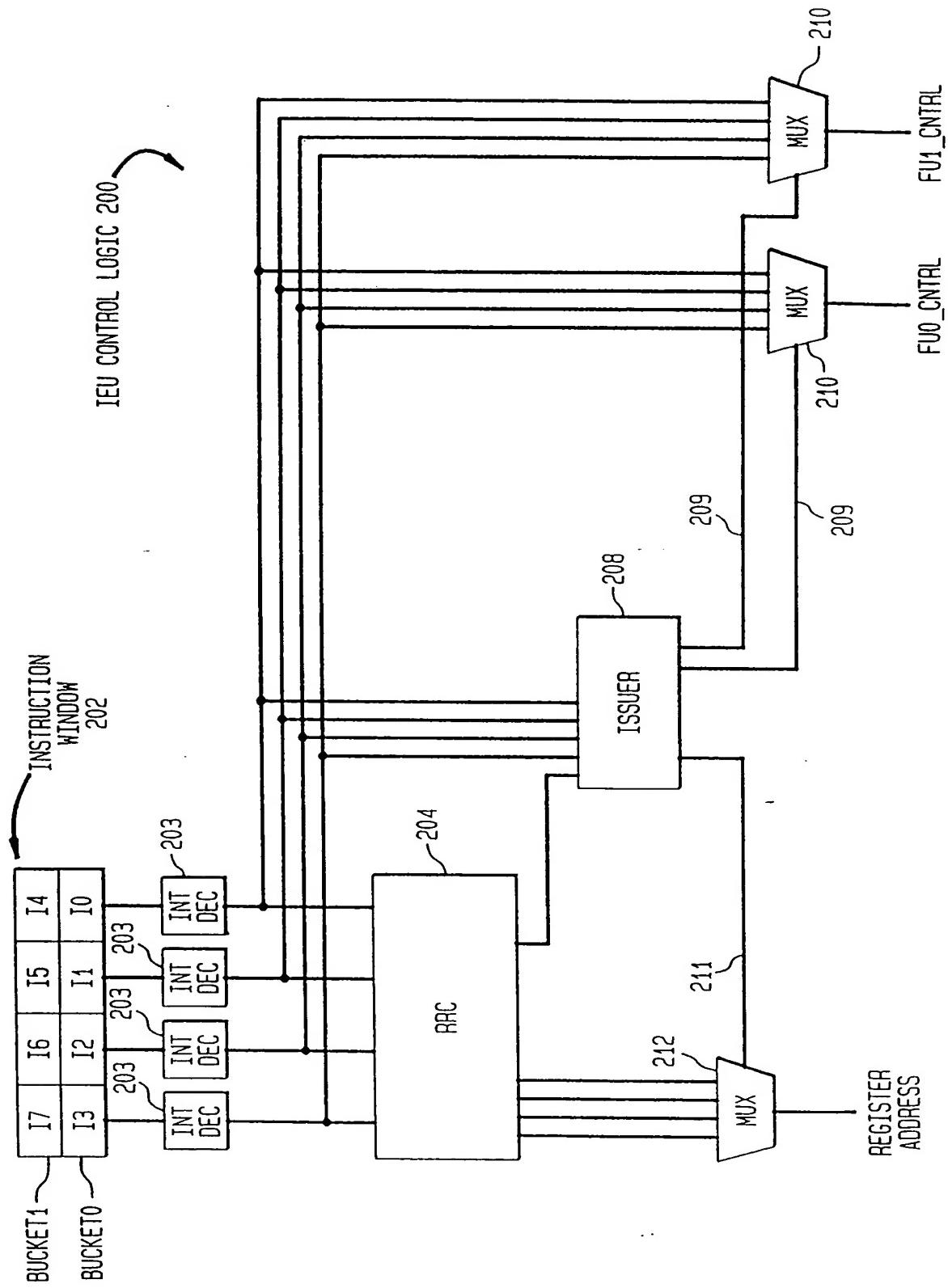


FIG. 2



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FIG. 3

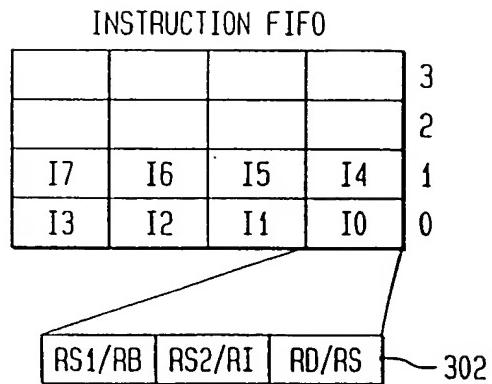


FIG. 5A

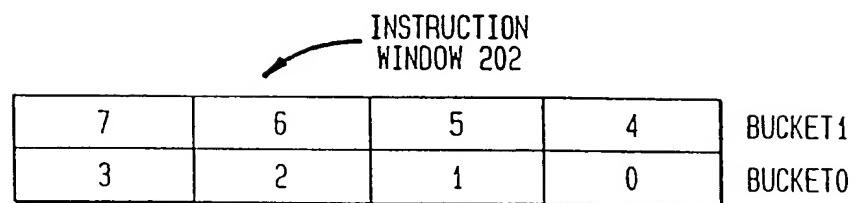


FIG. 5B

TEMPORARY BUFFER 403

7	I3RD+1	OR	I7RD
6	I3RD		
5	I2RD+1	OR	I6RD
4	I2RD		
3	I1RD+1	OR	I5RD
2	I1RD		
1	I0RD+1	OR	I4RD
0	I0RD		

The diagram shows a temporary buffer with 8 stages. Stage 0 contains I0RD, stage 1 contains I1RD, stage 2 contains I1RD, stage 3 contains I0RD+1, stage 4 contains I2RD, stage 5 contains I2RD+1, stage 6 contains I3RD, and stage 7 contains I3RD+1. An arrow points from the buffer to a label TEMPORARY BUFFER 403.

FIG. 4

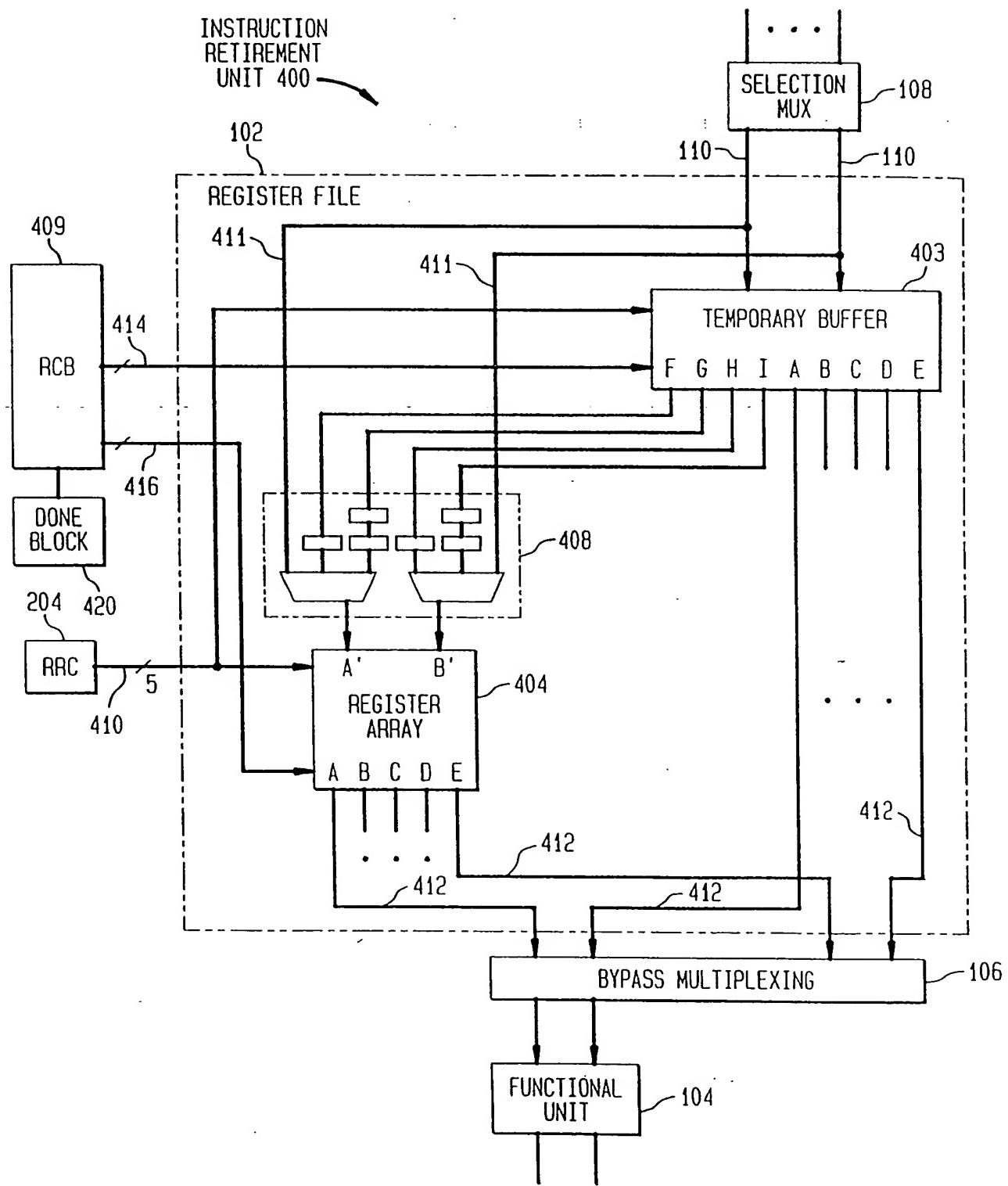


FIG. 6A

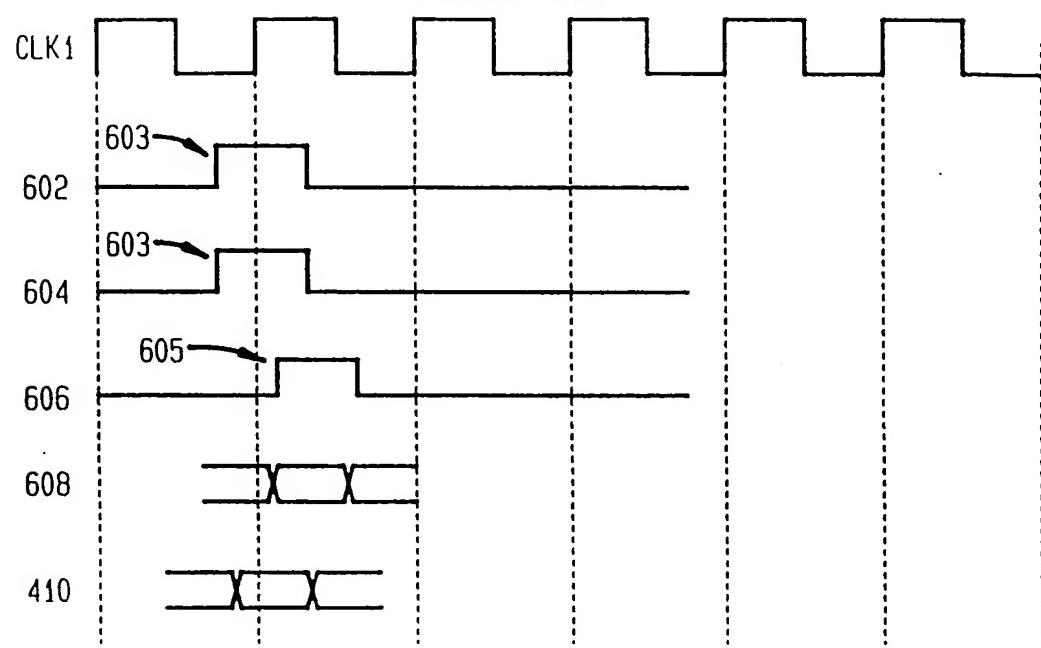


FIG. 6B

